

DERWENT-ACC-NO: 2002-555444

DERWENT-WEEK: 200259

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TITLE: Method for forming trench isolation  
layer of semiconductor device

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PATENT-FAMILY:

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KR 2002014538 A		February 25, 2002	N/A
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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
KR2002014538A	N/A	2000KR-
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INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: KR2002014538A

BASIC-ABSTRACT:

NOVELTY - A method for forming a trench isolation layer of a semiconductor device is provided to prevent the profile of an active region from being deteriorated by a silicon selective epitaxial growth(SEG), by performing a silicon SEG process in addition to a conventional shallow

**trench isolation(STI)**  
process.

DETAILED DESCRIPTION - A pad oxide layer(11) and a nitride layer are formed on a silicon substrate(10). The pad oxide layer and the nitride layer are patterned to form a trench in the silicon substrate by an isolation mask process and an etch process. An oxide layer(14) for filling the trench is formed on the resultant structure. The oxide layer is polished by using the nitride layer as a polishing stop layer. The nitride layer is removed, and the oxide layer is recessed low as compared with the silicon substrate in the active region. Silicon is laterally grown from the exposed silicon substrate by a SEG process. The pad oxide layer is removed.

CHOSEN-DRAWING: Dwg.1/10

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C01; L04-C06C; L04-C12C;

EPI-CODES: U11-C08A2;

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Basic Abstract Text - ABTX (1):

NOVELTY - A method for forming a **trench isolation** layer of a semiconductor device is provided to prevent the profile of an active region from being deteriorated by a **silicon** selective **epitaxial** growth(SEG), by performing a **silicon** SEG process in addition to a conventional shallow **trench isolation(STI)** process.

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